

Characterization of new materials for capacitor formation in integrated circuit technology

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Introduction

There have been tremendous developments in electronic technology in the last 40 years as evidenced by the widespread availability of computers, mobile phones and electronic entertainment systems and their continued shrinking in size and cost.

Much of the improvement in the performance of electronic systems can be traced to developments in Integrated Circuits (ICs) (“microchips”) which form the fundamental building blocks of modern electronics technology. Within an IC, the most important electronic component is the transistor and it is the transistor that is used to implement the operations associated with computer logic. With each generation of technology, the size of the transistors is reduced and more of them can fit on a single IC, which allows more powerful devices to be made that take up the same or even smaller space and draw less power from the battery. This trend regarding the scaling down in size of the transistors was first noticed by Gordon Moore, the co-founder of Intel, in 1965 and has since come to be known as Moore’s law. This states that “the number of transistors that can be placed on an integrated circuit (of a given area) doubles approximately every two years”. This law is expected to hold until at least the year 2015 if not longer.

While it is the transistors on an IC that implement the computer logic and other functions, they are not enough by themselves to form a complete system. Several other types of electronic components must also be placed on an IC to make the overall system perform a useful function. One of these components is known as the capacitor. A capacitor is similar to a battery in the sense that it can store electrical charge. Capacitors are widely used in electronic systems to help maintain a constant high-quality power supply to the rest of the electronics, as part of the tuning elements in radios and other wireless devices and for a variety of other purposes. With each new generation of IC technology, capacitors have to shrink in size, just like the transistors, so that the benefits of scaling can continue to be exploited. The research presented in this paper supports the continued scaling of capacitor components by developing techniques to characterize the performance of advanced

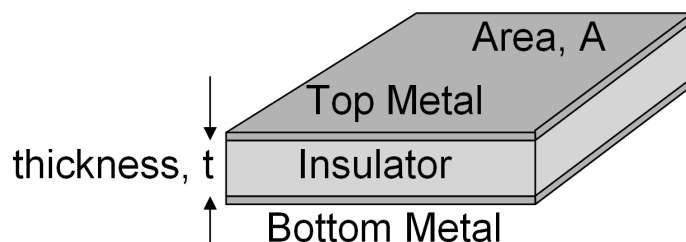


Figure 1: MIM capacitor

new materials that can be used to make small, high performance capacitors for future generations of IC technology.

Integrated Circuit Capacitors

Most of the high performance capacitors on an IC are made using a simple 3-layer sandwich structure like that illustrated in Figure 1.

The two outer layers of the capacitor sandwich are made of a metal such as copper (Cu) or aluminium (Au). Copper is a very good conductor, i.e. it allows electrical current to pass along it easily, which is why it is used extensively for electrical wiring in buildings. Aluminium is also a very good conductor and has some properties which make it easier to use for IC fabrication than copper. The middle layer of the 3-layer sandwich is made of an insulator material. The insulator, also commonly known as the dielectric, acts as a barrier to the flow of electrical current between the two metal layers and the combination of the three layers gives rise to the charge storage properties of the capacitor structure. This type of capacitor is commonly referred to as a parallel-plate MIM capacitor because of the Metal-Insulator-Metal arrangement of the layers. Until recently, silicon dioxide (chemical symbol SiO_2) has been the most widely used material for making insulator layers in integrated circuits. The SiO_2 layers on an IC are of extremely high purity and are made under precisely controlled temperature and pressure conditions during the IC manufacturing process. SiO_2 also occurs in nature where it is commonly called silica and occurs as sand and quartz.

A very important characteristic of a capacitor is its capacitance which is a measure of how much electrical charge it can store for a given voltage applied across the two metal layers. The capacitance of a parallel-plate MIM capacitor such as that shown in Figure 1 is given by Equation 1:

$$C = \frac{\epsilon_0 \epsilon_r}{t} A \quad (1)$$

Equation 1 shows that the capacitance depends on the dimensions of the capacitor and the properties of the insulator material. The important dimensions are the area of the capacitor (A) and the thickness of the insulator layer (t). The capacitance increases if

the area, A , is increased or if the insulator thickness, t , is reduced. The capacitance also depends on a physical constant, ϵ_0 , which does not change with technology, and a property of the insulator material called the dielectric constant, ϵ_r . The value of ϵ_r for the most commonly used dielectric, silicon dioxide, is approximately 3.9. With each new generation of technology there is a demand to reduce the size of the components to fit more of them into a single IC; thus, there is a demand to reduce the capacitor area, A . For many applications, the value of capacitance, C , must still be relatively large, however, if the area, A , has to be small, a large capacitance, C , can still be achieved by making the insulator layer thinner, i.e., by reducing the value of t . In present generation technologies, the area, A , can vary from several square microns to thousands of square microns (one micron is one millionth of a metre; for comparison purposes a micron is approximately equal to 1/100 of the diameter of a human hair), while the thickness, t , can vary from several nanometres to several hundred nanometres, where a nanometre (nm) is equal to one billionth (1/1,000,000,000) of a metre. Unfortunately, if the thickness, t , is too small, leakage current can flow across the dielectric layer and the dielectric no longer has perfect insulation. This can cause the integrated circuit to operate incorrectly or to consume too much battery power and, therefore, there is a limit to how thin the dielectric layers can be made.

Looking again at Equation 1, if a large value of capacitance, C , is required but if the area, A , must be kept small and there is also a limit to how small the thickness, t , can be made, then the only available option is to increase the value of the dielectric constant, ϵ_r . Therefore, in recent years, there has been extensive research into developing new types of materials that could be used to form the insulator layers of capacitors on integrated circuits and that would have a value of the dielectric constant, ϵ_r , higher than that of silicon dioxide. These new materials are commonly called “high-k” materials because the symbols “k” and “ ϵ_r ” are often used interchangeably.

High-k Materials

Many new materials have been proposed to meet the challenges of high-quality insulator layers for capacitors in IC technology over the next decade. To meet these challenges, any new material must meet stringent performance specifications such as being a very good insulator, having a high value of the dielectric constant (k , ϵ_r), and being compatible with all the other steps of the integrated circuit manufacturing process. The development of new materials therefore involves extensive research on all aspects of the material such as the chemical composition, the physical structure, the methods used to process the material during IC fabrication and the characterization of the electrical properties of the material such as the dielectric constant. Over the last 4 years, a team of scientists and engineers at the Tyndall National Institute in collaboration with partners from other

European organizations have developed processing techniques and measurement (characterization) methods to explore a promising new type of material suitable for capacitors known as PMNT. PMNT is a ceramic-type material made from a compound of the elements lead, magnesium, niobium, titanium and oxygen with a chemical composition given by $\text{Pb}(\text{Mg}_{0.33}\text{Nb}_{0.67})_{0.65}\text{Ti}_{0.35}\text{O}_3$. It has been demonstrated that PMNT can yield an extremely high dielectric constant of over 1000 (compared to 3.9 for silicon dioxide) and therefore has great potential for making large-value capacitors for IC technology.

Most integrated circuits used in modern electronic devices are made from silicon (Si) and are usually processed as thin wafers (that look similar to pizzas) with a thickness of 0.5 mm or less and a diameter ranging from 8 inches to 12 inches. The manufacturing process begins with wafers of high purity silicon and in each step of the manufacturing process new layers are grown on top of the original wafer to gradually build up all the components needed to form the desired electronic circuit. For the PMNT processes developed in this research, the PMNT layer is created on the silicon wafers in a multi-step process. First, the PMNT material is prepared in the form of a liquid gel. A droplet of this gel is dropped onto the centre of the silicon wafer and then the wafer is spun at very high speeds to cause the droplet to spread out over the surface of the wafer in a very thin layer. At this stage, the PMNT is still in a liquid form and must now be transformed into a strong solid layer. This is achieved by a process called annealing, where the wafer is heated to a high temperature (hundreds of degrees Celsius) at which the final chemical reactions occur and the material changes to a solid form. In IC manufacture, each of the steps of the process must be carried out at a precisely controlled temperature to ensure that the layers grown will have the desired chemical composition and physical structure. There is also a constraint that, as each layer is processed, the layers created earlier should not be physically damaged or changed in chemical composition. One of the most common ways of damaging a layer created earlier is to use too high a temperature in a subsequent step; therefore, the temperatures needed for the annealing step during the creation of the PMNT layers is of critical importance and is one of the main aspects investigated in the research. To determine the influence of temperature, samples were prepared using different annealing temperatures and the samples were then analysed to determine the influence of temperature on the electrical performance, especially the dielectric constant.

Electrical Performance of PMNT Capacitors

A set of special test structures were designed to allow sample capacitors to be made with the new material PMNT as the dielectric layer. To investigate the effect of annealing temperature, two sets of samples were processed. The first set of samples used an annealing temperature of 450°C for the PMNT layer and the second set of samples using a temperature of 750°C — these samples are labelled as PMNT_450 and PMNT_750, respectively.

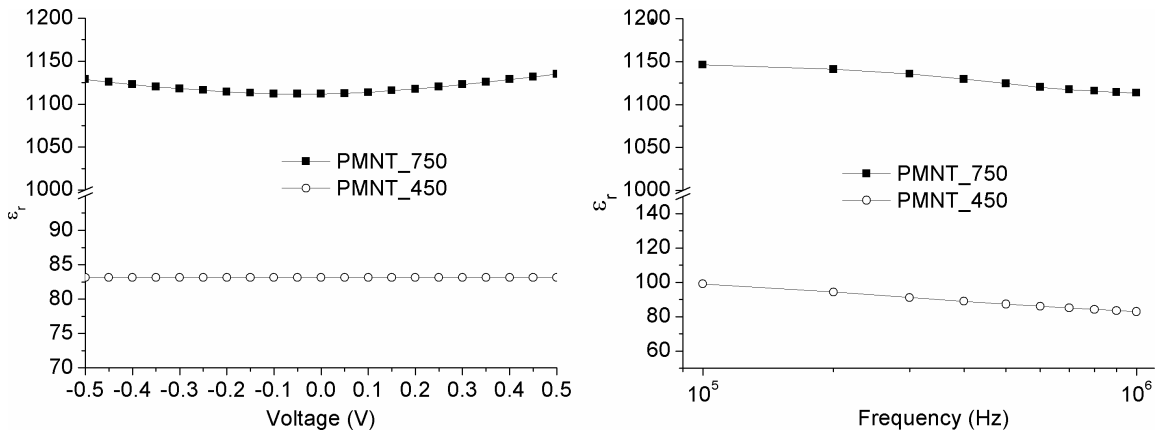


Figure 2: (a) The dielectric constant of the PMNT MIM capacitors as a function of voltage; (b) The dielectric constant of the PMNT MIM capacitors as a function of frequency.

When processing was complete, the capacitance of the capacitors was measured using a standard high-quality capacitance measurement system and the measured capacitance was used to determine the value of the dielectric constant, ϵ_r , of the PMNT layers, by a suitable rearrangement of Equation 1.

Apart from the having a high dielectric constant, ϵ_r , there are many other desirable attributes for the material making up the middle insulator layer of MIM capacitors, but two attributes are especially important; first, the value of the dielectric constant should not change with the voltage applied to the capacitor, and, second, the value of the dielectric constant should not change with the frequency of the electronic signal applied to the capacitor. Both of these attributes have been analysed for the PMNT samples developed in this research and are shown in graphical format in Figure 2.

Figure 2 illustrates the most important characteristics of the PMNT layers for the purposes of making high-quality capacitors. The most important aspect to notice from the figure is the difference between the samples annealed at 450°C and 750°C. It is seen that the dielectric constant of the samples processed at 750°C is much higher (approximately 1000) than the samples processed at 450°C (approximately 100). This indicates that for high-value capacitors, the PMNT material needs to be annealed at the higher temperature. The other important aspect to notice from the graph is that the dielectric constant of the PMNT does not vary significantly with either the voltage applied to the capacitor or the frequency of the signal used. Both these aspects indicate good performance and point to the good potential of the PMNT material to be used for capacitors in future generation integrated circuits.

Conclusion

This research has focused on the development of measurement strategies for a new type of material known as PMNT for use in future generations of integrated circuit technology as the insulator layer of high-performance Metal-Insulator-Metal capacitor devices. A set of capacitor test structures have been designed and samples have been processed under different conditions to determine the effect of annealing temperature on the electrical characteristics of the final capacitors. It has been shown that the PMNT material displays a very high dielectric constant (high-k) (approximately 1000, compared to 3.9 for SiO₂, the most commonly used dielectric in the current generation of IC technology), but in order to achieve this very high value, a high annealing temperature is necessary. Thus, PMNT is a very promising material for future use in ICs, especially if the annealing temperatures needed to give the high-k performance can be reduced.

Wenbin Chen is a student at the Tyndall National Institute under the supervision of Dr. Kevin G. McCarthy and Dr. Alan Mathewson. Co-authors Alan Mathewson, Mehmet Çopurođlu, Shane O'Brien, and Richard Winfield are based at the Tyndall National Institute and Kevin McCarthy is a lecturer in the Department of Electrical and Electronic Engineering. The authors would like to acknowledge the European Union Sixth Framework Programme for funding this research through STREP Project 033103 (CAMELIA). Wenbin Chen also receives support from the PRTL1 4 project NEMBES.